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Electrical Stability of Advanced a-Si:H TFT Structures

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Abstract In this paper, we study current-temperature stress (CTS) induced electrical instability of fork, Corbino and hexagonal (HEX) shaped hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) structures. We first investigate asymmetrical bias-dependent electrical instabilities of fork and Corbino TFTs. For HEX TFTs, influence of a threshold voltage shift of a single-HEX TFT on the overall electrical performance of multiple-HEX TFTs is discussed. The HEX TFTs show an improved electrical stability and threshold voltage shifts linearly with the number of connected basic HEX-units.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been extensively used as pixel circuits for large-area flat-panel displays and X-ray imagers due to excellent spatial uniformity and low fabrication cost [1,2]. To use such devices for active-matrix organic light-emitting diodes (AM-OLEDs) and various analog amplifiers and switches, a higher drain current and better electrical stability under prolonged bias stress are required [3,4]. For a given channel length of a standard TFT, a higher drain current can be achieved by increasing the TFT channel width using advanced TFT structures such as fork, Corbino or hexagonal (HEX) a-Si:H TFTs [6-8]. Corbino and hexagonal (HEX) a-Si:H TFTs proposed by *Lee et al.* provide a larger pixel aperture ratio compared to a standard TFT's for a given channel width. Moreover, the a-Si:H HEX TFT current level can be adjusted to a desirable value by connecting a number of HEX TFTs in parallel [8].

It is known that TFTs with asymmetric source-drain electrode have a better electrical stability compared to a standard TFT for a same channel width to length (*W/L*) ratio at a proper bias condition [9,10]. To assess potential of fork, Corbino and HEX TFTs for future flat panel displays, it is essential to evaluate their electrical stability. In this paper, we report detailed studies of the current-temperature stress (CTS) induced electrical instability of these advanced TFT structures. We first studied asymmetrical bias-dependent threshold voltage shift (ΔV_{th}) of fork and Corbino TFT. Then we measured ΔV_{th} of single HEX-TFTs and investigated their contribution to overall ΔV_{th} of multiple HEX-TFTs.

2. Fabrication

Fork, Corbino and hexagonal a-Si:H TFTs were fabricated using the normal AM-LCD 5-photomask process steps (Fig. 1). All multiple HEX TFTs were based on identical single HEX TFTs, whose gate, drain, and source electrodes are connected in parallel, respectively. On the Corning Eagle2000 glass substrate, bi-layer of molybdenum (Mo, 500Å) and aluminum-neodymium alloy (AlNd, 2000Å) was deposited by a sputtering method. The

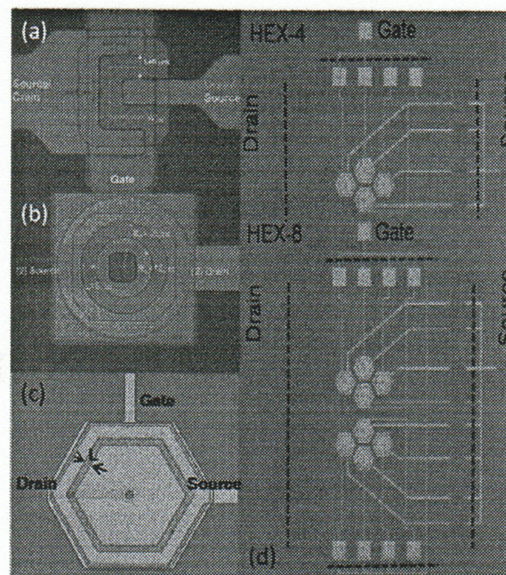

Fig.1. Photographs of fabricated (a) fork (b) Corbino (c) Single-HEX, and (d) Multiple-HEX a-Si:H TFTs.

Mo/AlNd gate electrode was then patterned by wet-etching (Mask#1). Following gate electrode definition, hydrogenated amorphous silicon nitride (a-SiN_X:H, 4000 Å) / a-Si:H (1700 Å) / phosphor-doped a-Si:H (n^+ a-Si:H, 300 Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200 Å) layer was deposited by sputtering, and source/drain (S/D) electrodes were patterned by wet-etching (Mask #3). Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN_X:H (3000 Å) as a passivation (PVX) layer by PECVD at 300 °C. To realize an electrical contact to electrodes (source/drain and gate), vias were formed through the PVX layer by RIE (Mask #4). After contact vias definition, ITO (500 Å) was deposited by a sputtering method at room temperature, and then

pixel electrodes and probing pads were patterned by wet-etching (Mask #5). As a final step, the thermal annealing was performed for an hour at 235 °C.

3. Experiments

A series of CTS measurements of fork, Corbino, and single- and multiple-HEX TFTs were performed using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature (T_{STR}) at 80 °C. The total stress time (t_{STR}) was 10,000 sec, and we only interrupted the applied stress for 60 sec to measure the transfer characteristics. During the CTS measurements, we connected the gate and drain bias together and so the TFTs operate in saturation regime. We continuously applied the current through drain bias to the TFTs.

To show asymmetrical electrical properties of fork TFT, we first measured the output characteristics under different bias conditions; (1) drain bias to U-shaped electrode and source to rod-shaped electrode, (2) drain bias to rod-shaped electrode and source to U-shaped electrode (Fig. 2). The output current is not symmetric for the same V_{DS} and V_{GS}; I_{DS} for a case (2) is about 1.5 times higher than for other case (1). Detailed studies on this subject can be found in [6]. Corbino and HEX TFTs also show this asymmetrical electrical property [7-8]. Both source-drain bias connections are used in CTS measurement of fork and Corbino TFTs.

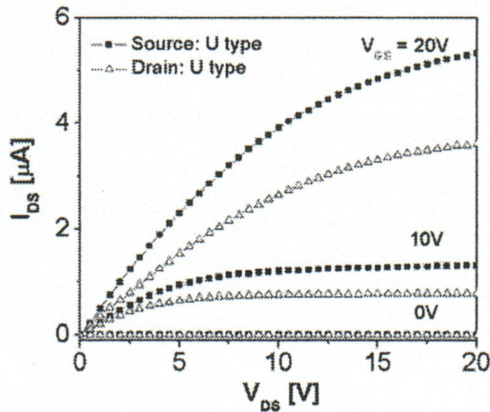

Fig. 2. Asymmetrical output characteristics of the fork a-Si:H TFT for various V_{GS}.

In HEX TFT measurement, drain and source bias were applied to inner and outer-electrode of the TFT, respectively, which allow achieving highest output current [8]. We applied different drain current values depending on the channel width to maintain the same stress current density (J_{STR} = 1667 A/cm^2) that corresponds to the OLED luminance of 10,000 cd/m^2 for the emission efficiency of 3.0 cd/A and the pixel size of 300 x 100 μm^2. For example, drain currents of 50, 100 and 167 μA were applied to HEX-1 (*W/L* = 300/5), HEX-2 (*W/L* = 600/5) and standard (*W/L* = 1000/6) a-Si:H TFTs, respectively.

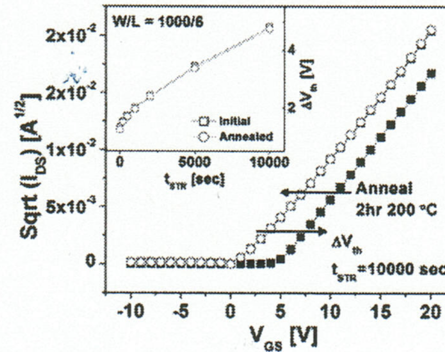

Fig. 3. The recovery of the CTS-induced I-V curve shift after thermal annealing is shown. The transfer characteristic is restored to its initial state after the annealing of 200 °C for 2 hours. (Inset) threshold voltage shift (ΔV_{th}) as a function of stress time (t_{STR}). Squares and circles represent the CTS results of the initial and the annealed TFT, respectively.

Using the same condition, we also measured independently all HEX-TFT basic units by cutting the parallel connection lines (Fig. 1). A standard TFT (*W/L* = 1000/6) was measured as well for comparison. We performed thermal annealing at 200 °C for 2 hour to ensure the consistent initial properties of the a-Si:H TFTs before each CTS measurement. Fig.3 shows that the CTS-induced stress could be fully recovered after each thermal annealing.

We extracted the threshold voltages using the maximum slope method over the stress time. The threshold voltage shift (ΔV_{th}) is defined as follows

$$\Delta V_{th}(t) = V_{th}\ (t = t_{STR}) - V_{th}(t = 0). \quad (1)$$

4. Result and Discussion

4.1. Asymmetrical Electrical Stability of Fork and Corbino TFT

Fig. 4 shows the asymmetrical ΔV_{th} with the stress current of the fork TFT for different source-drain bias connections induced by CTS. ΔV_{th} for case (2) is less than that for case (1). Although at low current stress (I_{STR} = 1 μA) their discrepancy is about 0.03 V, it increases to 0.14 V at I_{STR} = 4 μA. Similar asymmetrical ΔV_{th} is also observed for Corbino TFT (Fig. 5). The results imply that the discrepancy will become larger for a higher stress current density and a larger asymmetricity of source-drain electrode. When the fork and Corbino TFT are used as a switching TFT, source and drain bias connection may depend on its application and design. So understanding of this asymmetrical electrical instability is important.

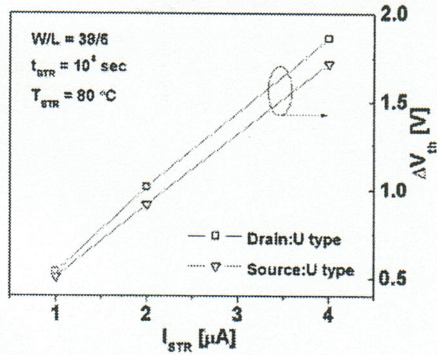

Fig. 4. Influence of the source-drain bias connection on ΔV_{th} for fork TFT under various stress current densities. I_{STR} of 1, 2, and 4 μA corresponds to J_{STR} of 263, 527 and 1053 A/cm^2, respectively.

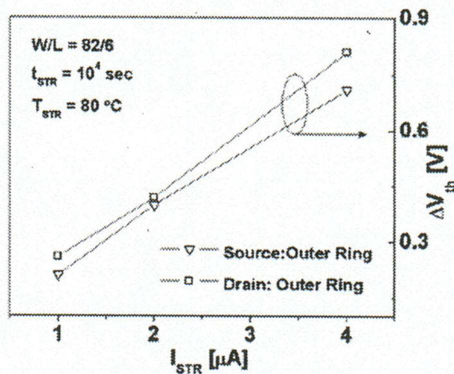

Fig. 5. The influence of the source-drain bias connection on ΔV_{th} for Corbino TFT under various stress current densities is shown. I_{STR} of 1, 2, and 4 μA corresponds to J_{STR} of 122, 244 and 488 A/cm^2, respectively.

4.2. Electrical Stability of Single- and Multiple-HEX TFTs.

Fig. 6 shows the ΔV_{th} variation as a function of stress time (t_{STR}) for different TFTs studied in this work. The ΔV_{th} of HEX-2 (W/L = 600/5), HEX-4 (W/L = 1200/5) and HEX-8 (W/L = 2400/5) are 3.26 V, 3.56 V and 3.82 V, respectively. The result of the standard TFT is shown for comparison.

ΔV_{th} increases with W/L ratio; larger width results in larger ΔV_{th} for a given channel length (L = 5 μm). Because HEX-4 with even higher W/L ratio exhibited similar ΔV_{th} to standard TFT (W/L= 1000/6, ΔV_{th} = 3.55 V), parallel-connected multiple HEX-TFTs appear to have a better electrical stability (less ΔV_{th}) for the same W/L ratio compared to a standard TFT. Field-effect mobility (μ_{eff}) was also extracted from the transfer characteristics. The amount of μ_{eff} change ($\Delta\mu_{eff}$) after the CTS measurement for the standard TFT, HEX-2, HEX-4 and HEX-8 are 0.06, 0.07, 0.09 and 0.12 cm^2/(V·s), respectively.

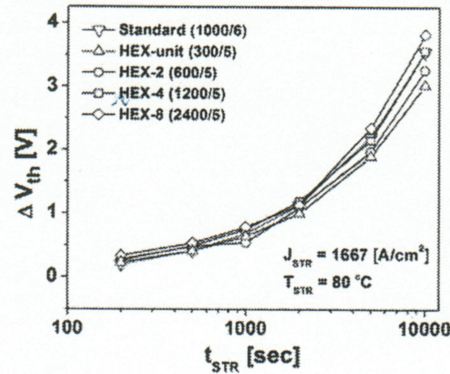

Fig. 6. Threshold voltage shifts (ΔV_{th}) of the single HEX-TFT unit, HEX-2, HEX-4 and HEX-8 TFT as a function of stress time (t_{STR}) in a semi-log scale.

The influence of ΔV_{th} of a single-HEX TFT on ΔV_{th} of multiple-HEX TFTs was also investigated. ΔV_{th} of all single-HEX TFTs for both HEX-4 and HEX-8 is 3.04 V ± 0.06. No specific single-HEX TFT dominates the overall circuit electrical instability as long as a-Si:H TFT process spatial uniformity control is adequate. We also estimated ΔV_{th} of parallel-connected multiple-HEX TFTs based on their unit device. ΔV_{th} of HEX-2^N TFT (N, integer) can be described by

$$\Delta V_{th_N} = \Delta V_{th_u} + N \times 0.27, \qquad (2)$$

where ΔV_{th_u} is ΔV_{th} of unit HEX-TFT and N is from HEX-2^N TFT.

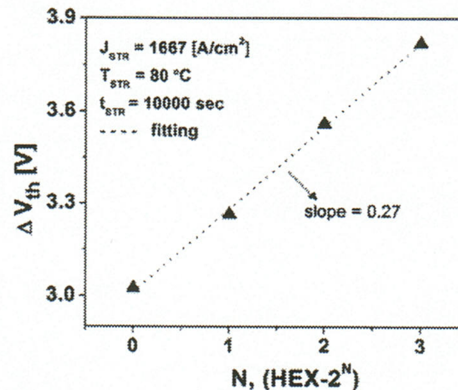

Fig. 7. CTS induced threshold voltage shift (ΔV_{th}) as a function of integer N of HEX-2^N; HEX-2^0 (W/L = 300/5), HEX-2^1 (W/L = 600/5), HEX-2^2 (W/L = 1200/5), and HEX-2^3 (W/L = 2400/5).

The linear relation between ΔV_{th} and number of unit TFTs can be explained as follows: for this specific experimental bias condition, ΔV_{th} is dominated by a combination of defect creation or/and charge trapping [11]. Indeed Fig. 3 shows power-law dependence

between ΔV_{th} and the stress time (t_{STR}). We observed $\Delta V_{th} \propto t_{STR}^{\beta}$, and β is extracted to be 0.65 ± 0.02. For a-Si;H TFT, the total channel charge (Q_{ch}) in the saturation region is given by [12]

$$Q_{ch} = 2/3 \cdot C_G \cdot W \cdot L\left(V_{GS} - V_{th}\right), \qquad (3)$$

where C_G is the gate capacitance per unit area, W the channel width, L the channel length, V_{GS} the gate-source bias.

The channel width increases with a number of parallel-connected HEX TFTs, and so does the total channel charge. For a larger Q_{ch} we expect that a larger number of carriers are available for either to be trapped at the silicon nitride/a-Si:H interface or/and to participate in breaking of Si-Si weak bonds to create charged Si defects. Both mechanisms will produce ΔV_{th} that is proportional to number of trapped charges. In other words, a larger number of trapped charges will result in a larger threshold voltage shift in agreement with the experiments.

4. Conclusion

We studied the electrical instabilities of fork, Corbino, and single-/multiple- a-Si:H HEX TFTs under the current-temperature stress. The fork and Corbino TFT show asymmetrical threshold voltage shift depending on the source-drain bias connection. The multiple-HEX TFTs show a better electrical stability compared to the standard TFT for similar *W/L* ratio. It is also found that one specific HEX unit in the multiple HEX-TFTs does not dominate or/and affect the overall TFT electrical instability. Furthermore, we established a relationship between the threshold voltage shift and number of units in the multiple HEX-TFT. The demonstrated electrical stability characteristics of advanced TFT structures need to be considered when used as a switching and/or driving TFT for flat panel display and other analog circuit applications.

Acknowledgments

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References

[1] R.A. Street, Ed., *Technology and Application of Amorphous Silicon*, New York: Springer-Verlag, 2000.

[2] N. Ibaraki, "a-Si:H TFT technologies for large-size and high-pixel density AM-LCDs," *Mater. Chem. Phys.*, vol. 43, No. 3, pp. 220-226, Mar. 1996.

[3] V.M. Da costa and R.A. Martin, "Amorphous silicon shift register for addressing output drivers," *IEEE J. Solid-State Circuits*, vol. 29, no. 5, pp. 596-600, May 1994.

[4] K.S. Karim, A. Nathan, and J.A. Rowlands, "Amorphous silicon pixel amplifier with ΔVT compensation for low noise digital fluoroscopy," *IEDM Tech. Dig.*, 2002, pp. 215-218.

[5] N. Matuski, Y. Abiko, K. Miyazaki, M. Kobayashi, H. Fujioka, and H. Koinuma, "Field-effect a-Si:H solar cells with transparent conductive oxide comb-shaped electrodes," *Thin Solid Films*, vol. 486, no.1/2, pp. 210-213, 2005.

[6] H. Lee, G. Yoo, J.-S. Yoo, and J. Kanicki, "Asymmetric electrical properties of fork a-Si:H thin-film transistor and its application to flat panel displays," *J. Appl. Phys*, vol.105, pp. 124522-1 – 124522-7, 2009.

[7] H. Lee, J.-S. Yoo, C-D. Kim, I.-B. Kang, and J. Kanicki, "Asymmetric electrical properties of Corbino a-Si:H TFT and concepts of its application to flat panel displays," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 654-662, 2007.

[8] H. Lee, J.-S. Yoo, C-D. Kim, I.-B. Kang, and J. Kanicki, "Hexagonal a-Si:H TFTs: a new advanced technology for flat panel displays," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 329-336, 2008.

[9] H.-Y. Tseng, K.-Y. Chiang, H.-Y. Lu, C.-P. Kung, and T.-C. Chang, "Layout dependence on threshold voltage instability of hydrogenated amorphous silicon thin film transistor," *J. Jpn. Appl. Phys.*, vol. 46, no. 3B, pp. 1318-1321, 2007.

[10] G. Yoo, H. Lee and J. Kanicki, "Electrical stability of hexagonal a-Si:H TFTs," *IEEE Electron Device Lett*, 2009 (doi: 10.1109/LED.2009.2034760)

[11] F.R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 62, pp. 1286-1288, 1993.

[12] Z. Tang, M.S. Park, S.H. Jin and C.R. Wie, "Drain bias dependent bias temperature stress instability in a-Si:H TFT," *Solid-State Electron.* vol. 53, pp. 225-233, 2009